

# Analysis and Control of Dual-Output LCLC Resonant Converters, and the Impact of Leakage Inductance

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**Abstract**—The analysis, design and control of 4<sup>th</sup>-order LCLC voltage-output series-parallel resonant converters (SPRCs) for the provision of multiple regulated outputs, is described. Specifically, state-variable concepts are developed to establish operating mode boundaries with which to describe the internal behaviour of dual-output resonant converters, and the impact of output leakage inductance. The resulting models are compared with those obtained from SPICE simulations and measurements from a prototype power supply under closed loop control to verify the analysis, modeling and control predictions.

## I. INTRODUCTION

To-date, several approaches have been explored to address cross-regulation, complexity and overall circuit performance issues of multi-output converters, the solutions being divided into three distinct categories. The first regulates a single primary output using closed-loop feedback, with the auxiliary outputs being semi-regulated and, therefore, subject to cross-regulation error. The second category achieves precise post-regulation of each output by using either linear regulators or hard-switched dc-dc converters. However, although relatively straightforward to design, such circuits are rarely used in practice due to cost constraints. The third category is specific to applications which require only two regulated outputs, as is commonly found in signal processing and microprocessor based systems. They avoid the need for post-regulation by utilising two closed-loop feedback configurations. A 3<sup>rd</sup>-order LLC converter with two independently controlled outputs was reported in [1]. However, optimum performance characteristics have yet to be forthcoming, primarily due to the significant complexity associated with the highly non-linear behaviour between the various outputs as a function of load. Nevertheless, it is a solution that broadly falls within this third category that is the subject of this paper. Specifically, dual-output resonant LCLC converters, are considered, with control of each output being achieved by switching the power devices asymmetrically over each half switching cycle using a combination of PWM and frequency control.

## II. DUAL O/P LCLC-SPRC MODEL

A half-bridge LCLC-SPRC with two outputs is shown in Fig. 1(a). To achieve zero-voltage switching, the converter is assumed to operate on the negative gradient of the input-output frequency characteristic, above the primary resonant peak. When operating in this region, the resulting waveforms can be

sub-divided into two distinct time intervals, viz. intervals 1 and 2, as depicted in Fig. 1(b):

**Interval 1:** Clamping of the parallel capacitor voltage. Here, the combined series inductor  $L_s$  (Fig.1(c)) and capacitor  $C_s$  provide resonant behaviour whilst the voltage across  $L_p$  and  $C_p$  is clamped by the output voltage. As the current through the series inductor,  $L_s$ , decays to zero,  $C_p$  begins to contribute to resonant behaviour, and operation enters the second interval.

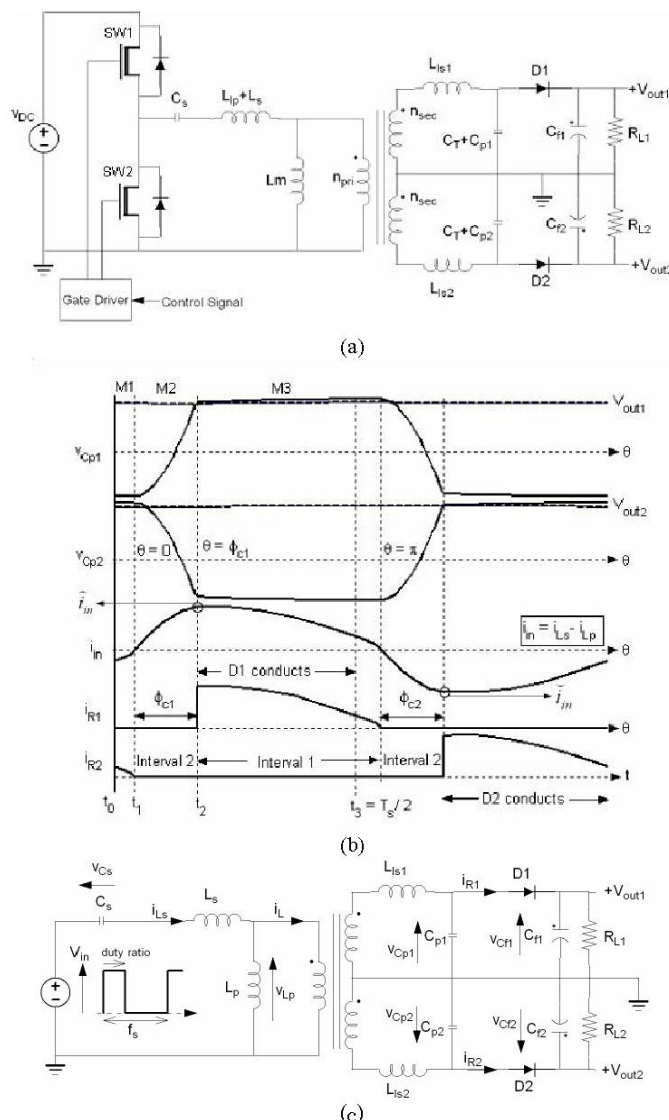


Fig.1 Dual-load 4<sup>th</sup>-order resonant converter (a) schematic (b) typical operating waveforms (c) simplified circuit

**Interval 2:** Decoupling of the rectifier and output filter. Here, all the tank components contribute to resonant behaviour, with the rectifier effectively becoming reverse biased. Current into both the high- and low-side diodes remains zero, and the parallel capacitors are charged until their voltage is clamped at either  $+V_{out1}$  or  $-V_{out2}$ , thereby providing the boundary at the end of this time interval. During each half-cycle of operation, three Modes, M1, M2, and M3 can be identified, as shown in Fig. 1(b).

**Circuit Mode M1** ( $t_0 \leq t < t_1$ ). At the start of M1, SW2 is turned off at  $t_0$  and SW1 turned on. The series inductor current,  $i_{Ls}$ , is negative and flows through the internal diode of SW1, thereby facilitating ZVS of SW1. Also during this period,  $i_{Ls}$  allows D2 to conduct and transfer energy to support  $V_{out2}$ , whilst the voltage on  $C_{p2}$  is clamped to  $V_{out2}$ . All the rectifier current, therefore, flows to the load. At the end of M1, the rectifier current  $i_{R2}$  has decayed to zero, and both the high side and low side diodes, and the output filter, are effectively decoupled from the resonant tank.

**Circuit Mode M2** ( $t_1 \leq t < t_2$ ). Here, the series resonant inductor current  $i_{Ls}$  becomes positive. Since SW1 is turned on during M1, current flow is now through SW1. Initial conditions for this mode are that  $i_{Ls}=0$  and  $v_{cp2} = V_{out2}$ . The inductor current  $i_{Ls}$  and parallel resonant capacitor voltages take on a sinusoidal characteristic. Since the outputs are effectively disconnected from the tank, both  $C_{p1}$  and  $C_{p2}$  contribute to resonant behaviour. Both rectifier currents are zero, and the converter outputs are in an 'idle' state, with energy being supplied solely by the charge on the filter capacitors. By initially neglecting the rectifier on-state voltage, and noting that the effective parallel resonant capacitance  $C_p$  is the sum of the shunt network capacitances  $C_{p1}$  and  $C_{p2}$ ,  $v_{cp1}$  during the capacitor charging period is described by:

$$v_{cp1}(t) = v_{cp1}(t_1) + \frac{1}{C_p} \int_{t_1}^t \hat{i}_{in} \sin(2\pi f_s t) dt \quad (1)$$

where  $\hat{i}_{in} = -(i_{Ls} - i_{Lp})$ . Evaluating (1) with initial conditions  $v_{cp1}(t_1) = v_{cp1}(t_1) = -V_{out2}$  yields:

$$v_{cp1}(t_2) = -V_{out2} + \hat{i}_{in} \times \frac{1 - \cos(2\pi f_s (t_2 - t_1))}{2\pi f_s C_p} \quad (2)$$

The boundary for the end of the capacitor charging period is  $v_{cp1}(t_2) = +V_{out1}$ , which yields the rectifier non-conduction angle,  $\phi_{c1}$ , associated with a positive polarity of current,  $i_{R2}$ , through the high side rectifier:

$$t_2 - t_1 = \frac{1}{2\pi f_s} \times \cos^{-1}(\phi_{c1}) \quad \phi_{c1} = \cos^{-1} \left( 1 - \frac{2\pi f_s C_p v_{tot}}{\hat{i}_{in}} \right) \quad (3)$$

where  $v_{tot} = V_{out1} + V_{out2}$ .

**Circuit Mode M3** ( $t_2 \leq t < T_s/2$ ). At  $t = t_2$ , D1 becomes forward biased whilst D2 reverse biased. The rectifier diode current  $i_{R2}$  remains zero throughout the duration of M3, and D1 clamps the capacitor voltage  $v_{cp1}$  to  $+V_{out1}$  until  $i_{Ls}$  decays to zero, at which time the second half cycle of operation commences.

For 50% duty-cycle excitation, the 2<sup>nd</sup> half-cycle of operation is the mirror image of the first. However, for asymmetrical excitation, the output rectifier diode (D2) non-conduction angle, associated with the series resonant inductor current being of negative polarity, is given by:

$$\phi_{c2} = \cos^{-1} \left( 1 - \frac{2\pi f_s C_p v_{tot}}{\hat{i}_{in}} \right) \quad (4)$$

where  $\hat{i}_{in} = i_{Ls} - i_{Lp}$ . The voltage,  $v_{cp1}$ , across the parallel resonant capacitor can, therefore, be expressed as a function of the angle  $\theta$ —see Fig. 1(b):

$$v_{cp1}(\theta) = \begin{cases} -V_{out2} + \frac{\hat{i}_{in}}{2\pi f_s C_p} \times (1 - \cos(\theta)) & \text{for } \theta = 0 \dots \phi_{c1} \\ +V_{out1} & \text{for } \theta = \phi_{c1} \dots \pi \\ V_{out1} - \frac{\hat{i}_{in}}{2\pi f_s C_p} \times (1 - \cos(\theta)) & \text{for } \theta = \pi \dots \pi + \phi_{c2} \\ -V_{out2} & \text{for } \theta = \pi + \phi_{c2} \dots 2\pi \end{cases} \quad (5)$$

Under steady-state conditions, the mean output current  $i_{out1}$ , flowing through D1 towards the output filter and load, can be determined from the mean current flowing through the rectifier when it is of positive polarity. Since this occurs during the interval  $\phi_{c1} \leq \theta < \pi$ ,  $i_{out1}$  is given by:

$$i_{out1} = \frac{1}{2\pi} \times \int_{\phi_{c1}}^{\pi} \hat{i}_{in} \sin(\theta) d\theta \quad (6)$$

Substituting (3) into (6) and evaluating the integral provides the solution for  $i_{out1}$ :

$$i_{out1} = \frac{\hat{i}_{in}}{2\pi} \times (1 + \cos(\phi_{c1})) = \frac{\hat{i}_{in} - \pi f_s C_p v_{tot}}{\pi} \quad (7)$$

Simple mathematical manipulation of (3) and (7) then gives the corresponding rectifier non-conduction angle  $\phi_{c1}$ :

$$\phi_{c1} = \cos^{-1} \left( \frac{\pi i_{out1} - \pi f_s C_p v_{tot}}{\hat{i}_{in} - \pi f_s C_p v_{tot}} \right) \quad (8)$$

$V_{out1}$  is determined by assuming the output filter capacitance  $C_f$  is sufficiently large to impart negligible output voltage ripple. In this case:

$$V_{out1} = i_{out1} R_{L1} = \frac{\hat{i}_{in} R_{L1}}{2\pi} \times (1 + \cos(\phi_{c1})) = \frac{R_{L1} (\hat{i}_{in} - \pi f_s C_p v_{tot})}{\pi} = \frac{R_{L1}}{\pi} \times \frac{\hat{i}_{in} - \pi f_s C_p V_{out2}}{1 + R_{L1} f_s C_p} \quad (9)$$

Equations (6) to (9) can be further manipulated to provide the complementary D2 non-conduction angle,  $\phi_{c2}$ , and the output current,  $i_{out2}$ , and output voltage  $V_{out2}$ , as follows:

$$i_{out2} = \frac{\tilde{i}_{in}}{2\pi} \times (1 + \cos(\phi_{c2})) V_{out2} = \frac{R_{L2}}{\pi} \times \frac{\tilde{i}_{in} - \pi f_s C_p V_{out1}}{1 + R_{L2} f_s C_p} \quad (10)$$

### III. STATE-VARIABLE ANALYSIS

A state-variable model describing the behaviour of the dual-output converter can be obtained by considering the electrical network shown in Fig. 1(c) and separating the dynamics into 'fast' and 'slow' sub-systems, with their interaction related by a set of coupling equations. The fast sub-system is considered to describe the dynamics of the resonant tank and power switches:

$$\begin{aligned} \frac{dv_{Cs}}{dt} &= \frac{i_{Ls}}{C_s}, \quad \frac{di_{Ls}}{dt} = \frac{V_{in} - v_{Cs} - v_{Lp}}{L_s}, \quad \frac{di_{Lp}}{dt} = \frac{v_{Lp}}{L_p} \\ \frac{dv_{Cp1}}{dt} &= \frac{i_{Ls} - i_{Lp} - i_{R1} - i_{Cp2} - i_{R2}}{C_{p1}}, \quad \frac{dv_{Cp2}}{dt} = \frac{i_{Ls} - i_{Lp} - i_{R2} - i_{Cp1} - i_{R1}}{C_{p2}} \end{aligned} \quad (11)$$

The output filter dynamics are described by:

$$\frac{dv_{cf1}}{dt} = \frac{i_{R1}}{C_{f1}} - \frac{v_{cf1}}{C_{f1}R_{L1}}, \quad \frac{dv_{cf2}}{dt} = \frac{i_{R2}}{C_{f2}} - \frac{v_{cf2}}{C_{f2}R_{L2}} \quad (12)$$

As discussed, during interval  $t_1 \rightarrow t_2$  (see Fig. 1(b))  $v_{Cp1}$  is clamped to  $v_{cf1}$  during the positive half-cycle, and conversely, to  $-v_{cf2}$  during the negative half-cycle, due to the action of the diodes. By noting that there will be negligible current flowing through  $C_p$  during these periods, the rectifier input voltage is dependent on the direction of the current leaving the resonant tank inductances, i.e.  $i_L = i_{Ls} - i_{Lp}$ . The relevant coupling terms are, therefore, obtained by equating voltages at either side of the rectifier for each respective half-cycle:

$$\begin{aligned} v_{Cp1} &= \text{sgn}(i_L)(V_{out1} + v_{diode}) = \text{sgn}(i_L)(v_{cf1} + v_{diode}) \\ v_{Cp2} &= \text{sgn}(i_L)(V_{out2} + v_{diode}) = \text{sgn}(i_L)(v_{cf2} + v_{diode}) \end{aligned} \quad (13)$$

Assuming a constant rectifier voltage, (12) can be manipulated to give:

$$\frac{dv_{Cp1}}{dt} = \text{sgn}(i_L) \frac{dv_{cf1}}{dt}, \quad \frac{dv_{Cp2}}{dt} = \text{sgn}(i_L) \frac{dv_{cf2}}{dt} \quad (14)$$

Considering the rectifier current,  $i_{R2}$ , to be zero during the positive half-cycle of the parallel capacitor voltage, the rectifier current  $i_{R1}$ , is given from:

$$\begin{aligned} \frac{i_L - i_{R1} - i_{Cp2} - i_{R2}}{C_{p1}} &= \text{sgn}(i_L) \left( \frac{i_{R1}}{C_{f1}} - \frac{v_{cf1}}{C_{f1}R_{L1}} \right) \\ \therefore i_{R1} &= \frac{C_{p1}C_{f1}}{\text{sgn}(i_L)C_{p1} + C_{f1}} \left( \frac{i_L - i_{Cp2} - i_{R2}}{C_{p1}} + \frac{\text{sgn}(i_L)v_{cf1}}{C_{f1}R_{L1}} \right) \end{aligned} \quad (15)$$

This leads to the following coupling equations which describe the rectifier currents within each half of a switching cycle:

$$\begin{aligned} i_{R1} &= \begin{cases} \frac{C_{p1}C_{f1}}{\text{sgn}(i_L)C_{p1} + C_{f1}} \left( \frac{i_L - i_{Cp2} - i_{R2}}{C_{p1}} + \frac{\text{sgn}(i_L)v_{cf1}}{C_{f1}R_{L1}} \right) & \text{for } v_{Cp1} = V_{out1} + v_{diode} \\ 0 & \text{for } v_{Cp1} < V_{out1} + v_{diode} \end{cases} \\ i_{R2} &= \begin{cases} \frac{C_{p2}C_{f2}}{\text{sgn}(i_L)C_{p2} + C_{f2}} \left( \frac{i_L - i_{Cp1} - i_{R1}}{C_{p2}} + \frac{\text{sgn}(i_L)v_{cf2}}{C_{f2}R_{L2}} \right) & \text{for } v_{Cp2} = V_{out2} + v_{diode} \\ 0 & \text{for } v_{Cp2} < V_{out2} + v_{diode} \end{cases} \end{aligned} \quad (16)$$

Notably, the voltage across  $L_p$  can be considered a reflection of the voltages across  $C_{p1}$  and  $C_{p2}$ , and the state vector for the parallel inductor current in the fast sub-system (see (11)) simplifies to  $v_{Lp} = v_{Cp}$ . The state-variable equations for the parallel resonant capacitor voltage (11) can be simplified to:

$$\frac{dv_{Cp1}}{dt} = \frac{i_{Ls} - i_{Lp} - i_R}{2C_{p1}}, \quad \frac{dv_{Cp2}}{dt} = \frac{i_{Ls} - i_{Lp} - i_R}{2C_{p2}} \quad (17)$$

The complete state-variable model of the dual load converter (excluding the effects of output leakage inductances) is, therefore, given by:

$$\dot{\mathbf{x}} = \begin{bmatrix} 0^{3 \times 3} & \mathbf{A}_1 & 0^{2 \times 3} \\ \mathbf{A}_2 & 0^{2 \times 2} & 0^{2 \times 2} \\ 0^{2 \times 3} & 0^{2 \times 2} & \mathbf{A}_3 \end{bmatrix} \mathbf{x} + \mathbf{B} \quad (18)$$

where

$$\begin{aligned} \mathbf{x} &= [v_{Cp1} \ v_{Cp2} \ v_{Cs} \ i_{Lp} \ i_{Ls} \ v_{cf1} \ v_{cf2}]^T \\ \mathbf{A}_1 &= \begin{bmatrix} -\frac{1}{2C_{p1}} & \frac{1}{2C_{p1}} \\ -\frac{1}{2C_{p2}} & \frac{1}{2C_{p2}} \\ 0 & \frac{1}{C_s} \end{bmatrix}, \quad \mathbf{A}_2 = \begin{bmatrix} \frac{1}{L_p} & 0 & 0 \\ -\frac{1}{L_s} & 0 & -\frac{1}{L_s} \end{bmatrix}, \quad \mathbf{A}_3 = \begin{bmatrix} -\frac{1}{C_{f1}R_{L1}} & 0 \\ 0 & -\frac{1}{C_{f2}R_{L2}} \end{bmatrix} \\ \mathbf{B} &= \begin{bmatrix} -\frac{i_R}{2C_{p1}} & -\frac{i_R}{2C_{p2}} & 0^{1 \times 2} & \frac{V_{in}}{L_s} & \frac{i_{R1}}{C_{f1}} & \frac{i_{R2}}{C_{f2}} \end{bmatrix}^T \end{aligned} \quad (19)$$

The model can be used to investigate the behaviour of dual load converters when subject to asymmetrical input excitation. By way of example, the parameters of a candidate converter are given in Table I when supplied from a 30V dc link. A plot of the resulting steady-state output voltage characteristics of the converter,  $V_{out1}$  and  $V_{out2}$ , as a function of switching frequency and duty-cycle ratio is given in Fig. 2. It is evident that for operation above resonance, the sum of the output voltages applied to the loads increases as the operating frequency tends to the effective resonant frequency, for fixed values of duty-cycle ratio. Furthermore, for a 50% duty-cycle, giving symmetric square-wave excitation of the tank, the converter delivers identical voltages to both the high side and low side outputs, for a fixed operating frequency, as expected. For a given operating frequency, a decrease in the duty-cycle ratio, from 50%, is seen to deliver more energy from the resonant tank to energize output  $V_{out1}$ , thereby yielding a correspondingly higher output voltage and power, and vice-versa. It is, therefore, clear that for balanced loads, the voltage and power distribution to each output can be independently influenced by a suitable choice of duty ratio and switching frequency.

TABLE I  
CONVERTER MODEL PARAMETERS

Parameters	Value
Characteristic impedance ( $\Omega$ )	2.5
Resonant inductance ratio, $L_n$	0.01
Resonant frequency, $f_o$ (kHz)	130
Resonant capacitance ratio, $C_n$	0.03
Series load quality factor, $Q_{opl}$	6

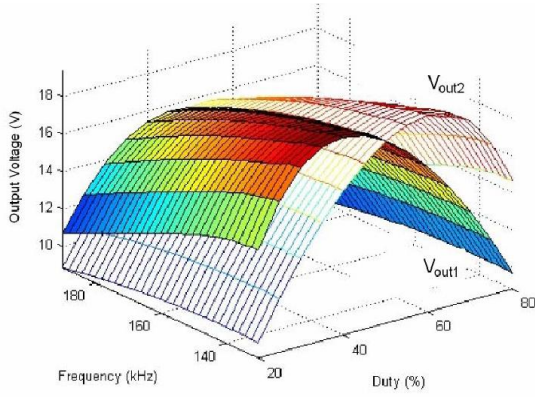


Fig.2 Variation of output voltage distribution with switching frequency and duty-cycle ratio

#### IV. IMPACT OF OUTPUT LEAKAGE INDUCTANCE

Although resonant converters are often designed to operate at relatively high frequencies, typically in the 200-500 kHz range, designers must still consider the impact of low levels of leakage inductance on converter performance. This is particularly evident for converters with multiple outputs, where the presence of such effects significantly complicates the analysis, particularly when determining the state of the parallel resonant inductor current,  $i_{Lp}$ , since the voltage seen across  $L_p$  cannot be assumed to be directly related to  $v_{Cp}$ , as a result of the voltages across the leakage inductances,  $L_{ls1}$  and  $L_{ls2}$ . The model must, therefore, be augmented with  $v_{Lp}$  to allow a solution for  $i_{Lp}$ . The converter can be separated into fast and slow sub-systems, Fig. 3 showing a model of the resonant converter ‘fast’ sub-system. Whilst the rectifier is omitted in the state-variable representation, its influence on the fast sub-system is accommodated through the addition of current sources, as shown in Fig. 3. This step is justified by noting that the interaction between the fast and slow sub-systems is solely based on coupling equations consisting of the characteristics of the rectifier output currents  $i_{R1}$  and  $i_{R2}$ . The slow sub-system describes the behaviour of the high side and low side rectifier outputs and the capacitive output filters and loads,  $v_{Cp1}$  and  $v_{Cp2}$  being considered to be the inputs to the high side and low side output sub-systems, respectively.

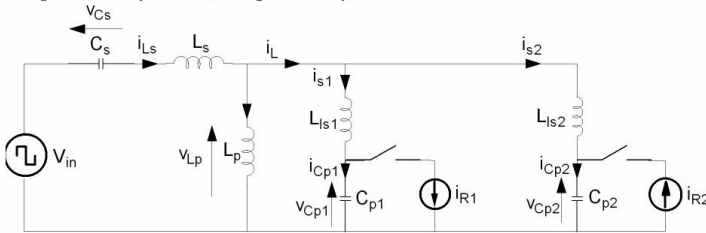


Fig. 3 State-variable representation of the fast sub-system.

The dynamics of the fast sub-system, therefore, consist of a set of state-variables whose value at time  $t = t_0$ , together with the input for all  $t > t_0$ , completely determines the behaviour of the system for any time  $t > t_0$ . An observable canonical state-space realization is, therefore, considered, as it allows the impact of parasitic elements to be readily included in the formulation, albeit at the expense of losing some of the physical

significance of the state-variables. The equivalent circuit in Fig. 3 is analyzed by considering each voltage and current source independently and using the principal of superposition to obtain the effective dynamic description for  $i_{Lp}$ :

$$\frac{di_{Lp}}{dt} = \frac{v_{Lp}}{L_p} = \frac{v_{Lp\_vi} + v_{Lp\_iR1} + v_{Lp\_iR2}}{L_p} = \frac{y_1 + y_2 - y_3}{L_p}$$

$$\dot{x}_1 = A_o x_1 + B_{o1} V_{in} \quad y_1 = v_{Lp\_vi} = C_o x_1 + D_{o1} V_{in}$$

$$\dot{x}_2 = A_o x_2 + B_{o2} i_{R1} \quad y_2 = v_{Lp\_iR1} = C_o x_2 + D_{o2} i_{R1}$$

$$\dot{x}_3 = A_o x_3 + B_{o3} i_{R2} \quad y_3 = v_{Lp\_iR2} = C_o x_3 + D_{o3} i_{R2}$$

where

$$A_o = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & -\frac{a_{13}}{a_{10}} \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -\frac{a_{12}}{a_{10}} \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & -\frac{a_{11}}{a_{10}} \\ 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}; \quad B_{c1} = \begin{bmatrix} -\frac{b_{10} \times a_{13}}{a_{10} \quad a_{10}} \\ 0 \\ -\frac{b_{10} \times a_{12} + b_{11}}{a_{10} \quad a_{10} \quad a_{10}} \\ 0 \\ -\frac{b_{10} \times a_{11} + b_{12}}{a_{10} \quad a_{10} \quad a_{10}} \\ 0 \end{bmatrix}; \quad B_{c2} = \begin{bmatrix} \frac{b_{22}}{a_{10}} \\ 0 \\ \frac{b_{21}}{a_{10}} \\ 0 \\ \frac{b_{20}}{a_{10}} \\ 0 \end{bmatrix};$$

$$B_{c3} = -B_{c2} \quad C_o = [0^{3 \times 1} \quad 1] \quad ; \quad D_{c1} = [1] \quad ; \quad D_{c2} = D_{c3} = [0]$$

$$b_{10} = L_p L_{ls1} L_{ls2} \quad b_{11} = \frac{L_p L_{ls1}}{C_{p2}} + \frac{L_p L_{ls2}}{C_{p1}} \quad b_{12} = \frac{L_p}{C_{p1} C_{p2}}$$

$$a_{10} = L_p L_{ls1} L_{ls2} + L_s L_p L_{ls2} + L_s L_p L_{ls1} + L_s L_p L_{ls2}$$

$$a_{11} = \frac{L_s L_{ls1}}{C_{p2}} + \frac{L_s L_{ls1}}{C_{p1}} + \frac{L_s L_p}{C_{p2}} + \frac{L_s L_p}{C_{p1}} + \frac{L_{ls1} L_{ls2}}{C_s} + \frac{L_p L_{ls2}}{C_s} + \frac{L_p L_{ls1}}{C_s} + \frac{L_p L_{ls1}}{C_{p2}} + \frac{L_p L_{ls2}}{C_{p1}}$$

$$a_{12} = \frac{L_s}{C_{p1} C_{p2}} + \frac{L_{ls1}}{C_s C_{p2}} + \frac{L_{ls1}}{C_s C_{p1}} + \frac{L_p}{C_s C_{p2}} + \frac{L_p}{C_s C_{p1}} + \frac{L_p}{C_{p1} C_{p2}} \quad a_{13} = \frac{1}{C_s C_{p1} C_{p2}}$$

$$b_{20} = L_s L_p L_{ls2} \quad b_{21} = \frac{L_p L_{ls2}}{C_s} + \frac{L_s L_p}{C_{p2}} \quad b_{22} = \frac{L_s}{C_s C_{p2}}$$

Adding the state vectors yields,

$$\dot{x}_1 + \dot{x}_2 + \dot{x}_3 = A_o (x_1 + x_2 + x_3) + [B_{o1} \quad B_{o2} \quad B_{o3}] \begin{bmatrix} V_{in} \\ i_{R1} \\ i_{R2} \end{bmatrix}$$

$$y_1 + y_2 + y_3 = v_{Lp\_vi} + v_{Lp\_iR1} + v_{Lp\_iR2} = C_o (x_1 + x_2 + x_3) + [D_{o1} \quad 0 \quad 0] \begin{bmatrix} V_{in} \\ i_{R1} \\ i_{R2} \end{bmatrix}$$

Now, by defining,  $x = x_1 + x_2 + x_3$  the observable canonical state-space equation simplifies to,

$$\dot{x} = A_o (x_1 + x_2 + x_3) + [B_{o1} \quad B_{o2} \quad B_{o3}] \begin{bmatrix} V_{in} \\ i_{R1} \\ i_{R2} \end{bmatrix}$$

$$y = v_{Lp} = C_o (x_1 + x_2 + x_3) + [D_{o1} \quad 0 \quad 0] \begin{bmatrix} V_{in} \\ i_{R1} \\ i_{R2} \end{bmatrix}$$

Substituting the output state, together with the coupling equations, leads to a steady-state solution of the model. The fast and slow sub-system models can also be combined and



used for implementation in simulation environments, eg. MATLAB<sup>®</sup>/SIMULINK.

## V. EXPERIMENTAL RESULTS

Measured results have been obtained on an experimental converter with a step-down capability, the measured component values being given in Table II. A ferrite core, 3F3, suitable for high frequency applications, was used for both the transformer core and the resonant inductor. Since the transformer leakage inductances are dependent on the winding arrangement, the secondaries were bifilar wound adjacent to the core, beneath the primary winding, so as to reduce secondary leakage flux.

TABLE II  
PROTOTYPE DUAL OUTPUT CONVERTER COMPONENT VALUES

Parameter	Value
DC link input voltage, $v_{DC}$ (V)	15
Series resonant inductances, $L_s$ ( $\mu$ H)	0.85
Series resonant capacitances, $C_s$ ( $\mu$ F)	1.5
High side parallel resonant capacitances, $C_{p1}$ ( $\mu$ F)	0.116
Low side parallel resonant capacitances, $C_{p2}$ ( $\mu$ F)	0.116
Load resistance, $R_L$ ( $\Omega$ )	4
Filter capacitance, $C_f$ ( $\mu$ F)	100
Magnetising inductance, $L_m$ ( $\mu$ H)	109
Transformer turns ratio	1
Transformer output leakage inductance, $L_{ls}$ ( $\mu$ H)	0.1
Transformer primary leakage inductance, $L_{lp}$ ( $\mu$ H)	0.7

The effective parallel resonant inductor is designed to be on the transformer primary side, such that  $L_p$  utilises the magnetising inductance,  $L_m$ , of the transformer. The effective series inductance comprises of the series inductor,  $L_s$ , and the primary leakage inductance,  $L_{lp}$ , and was measured as  $1.55\mu$ H. A comparison of the output voltage obtained from the state variable model, simulated to steady-state, with SPICE simulation results and measurements, is given in Fig. 4. As is clearly evident, the correlation between the theoretical predictions and the experimental data is extremely good. Moreover, a comparison of simulated and measured characteristics, when duty-cycle ratio control is employed, has also been obtained at an operating frequency of  $f_s=150$  kHz. The results are shown in Fig. 5 from which it can be seen that the proposed state-variable model provides sufficient accuracy for design and analysis purposes, the maximum error being  $<5\%$ .

## VI. CLOSED-LOOP CONTROL

The structure of the control methodology, which employs two decoupled feedback loops for independent control of frequency and duty-cycle ratio, is shown in Fig. 6. Parameters for the decoupled SISO controllers are chosen for good transient response and disturbance rejection. The digital compensator is tuned to respond quickly to variations of  $V_{out1}$ , whilst the controller reacting to variations of  $V_{out2}$ , acts relatively slowly, thereby allowing an effective decoupling of the control loops, for simplicity. The prototype converter controller is shown in Fig. 7. The converter (see Table II for parameters) is required

to provide regulated  $+5V$  and  $+3.3V$  outputs from a DC link input voltage in the range  $15V$  to  $20V$ . Figure 8 shows the steady-state error between the reference voltages,  $V_{ref1}$  and  $V_{ref2}$ , and the resulting measured output voltages of the converter, over the specified range of DC link input voltages ( $15V$  to  $20V$ ) with a  $5\Omega$  load.

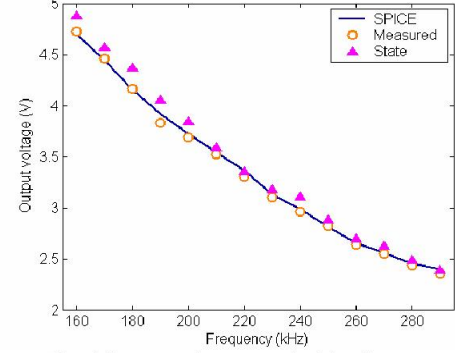


Fig. 4 Output voltage vs switching frequency

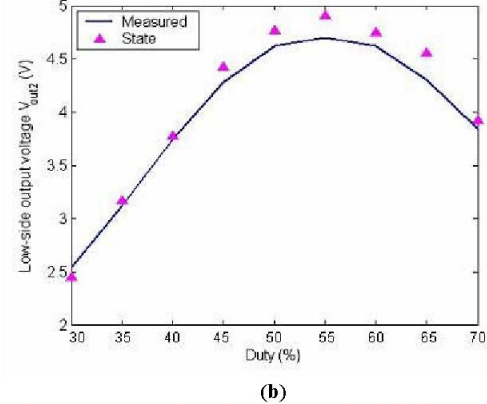
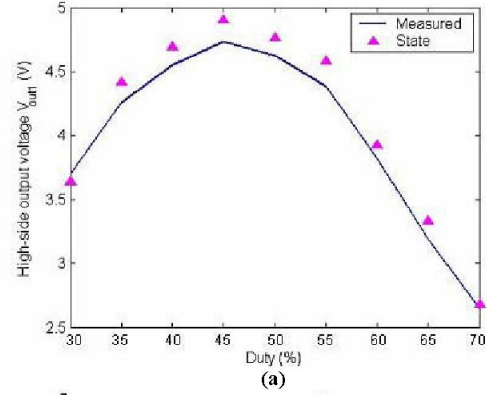


Fig. 5 Control characteristic curves for  $f_s=150$  kHz (a) high side output, and (b) low side output.

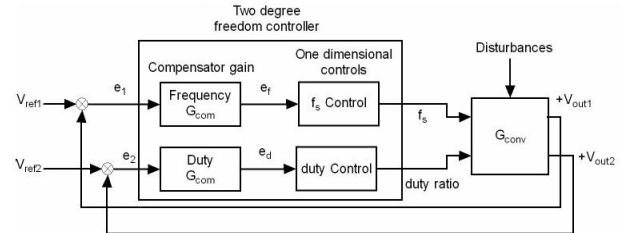


Fig. 6 Closed-loop control of the dual-load converter.

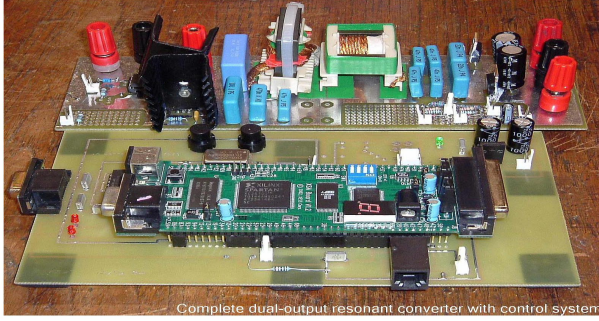


Fig. 7 Digital control of dual-output converter.

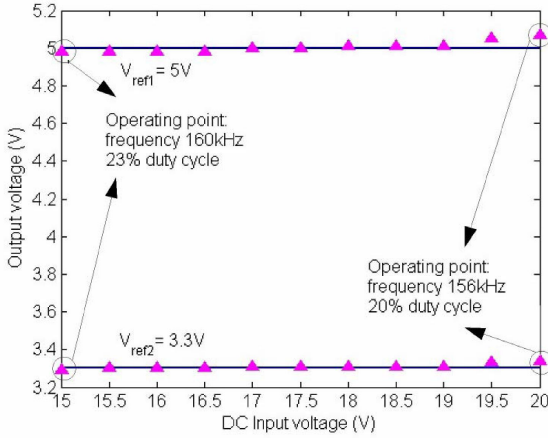
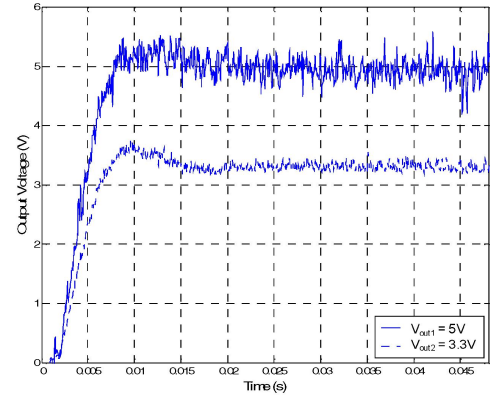


Fig. 8 Output voltage regulation vs. input voltage

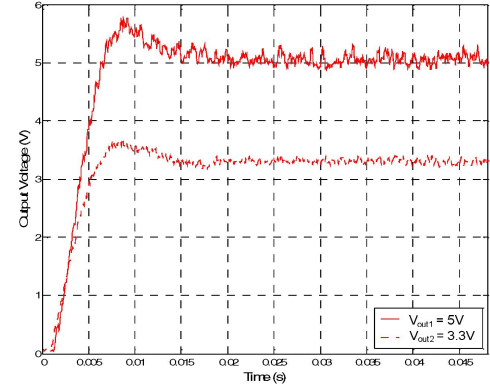
It can be seen that the maximum regulation error for both outputs is  $<5\%$ . Finally, Fig. 9 shows the response of the converter resulting from transient start-up conditions, for a range of applied input voltages and dual output voltage ratios. It can be seen that the converter voltages converge rapidly to the reference values, with an initial overshoot of  $\sim 10\%$ , corresponding to an equivalent  $2^{\text{nd}}$ -order damping ratio of  $\zeta \approx 0.6$ .

## VII. CONCLUSIONS

The characteristics of dual-load,  $4^{\text{th}}$ -order LCLC voltage-output resonant converters, have been explored. From the output voltage distribution derived from an example converter, the impact of the converter design parameters, and output leakage inductance, on the attainable output voltage ratio, has been investigated. A comparison of measurements from an experimental converter, capable of delivering 5V and 3.3V, with predictions from the derived state-variable model and SPICE simulations, shows that the state-variable model provides accurate predictions of output voltage under steady-state conditions. Moreover, a basic control scheme to allow reliable regulation of both outputs, has been realised, with steady-state measurements showing independent regulation using a combination of duty-cycle and frequency control, and good start-up transient behaviour on both outputs under a range of operating conditions.



(a)



(b)

Fig. 9 Start-up transient response for various dual output voltage ratios and DC-link input voltages (a)  $v_{DC}=15V$ ,  $V_{out1}=5V$ ,  $V_{out2}=3.3V$ ; (b)  $v_{DC}=20V$ ,  $V_{out1}=5V$ ,  $V_{out2}=3.3V$

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